CLAIMS

1. A method of accessing the testing means in a Field Programmable Gate Array ("FPGA") comprised of a plurality of functional groups ("FGs") comprising:

inputing a function netlist defining a user circuit;

compiling said function netlist;

generating a logic Built-In Self Test ("BIST") netlist.

2. The method of claim 1 further comprising extracting scan chain from said logic BIST netlist and predicting an expected syndrome value.

3. The method of claim 2 further comprising applying said scan chain to the FPGA and obtaining actual syndrome values.

4. The method of claim 3 further comprising:

comparing said expected syndrome values with said actual syndrome values; and

flagging error if said expected values are different than said actual values.

5. A method of accessing the testing means in a FPGA comprised of a plurality of functional groups comprising:

inputing a function netlist defining a user circuit;

optimizing said user circuit;

placing user cells into said FPGA functional unit;

defining routing structure to interconnect said functional units to implement said user circuit;

generating a programming bitstream;

programming said FPGA functional unit with said bitstream;

generating a BIST netlist;

extracting scan chain from said BIST netlist and predicting an expected syndrome value;

apply scan chain to FPGA and obtaining the actual syndrome values;

comparing said expected syndrome values with said actual syndrome values; and

flagging error if said expected values are different than said actual values.

6. An apparatus for accessing the testing resources in a programmed FPGA employing internal scan chains comprising:

means for generating a BIST netlist;

means for extracting a scan chain from said BIST netlist and predicting an expected syndrome value;

means for applying said scan chain to FPGA and obtaining actual syndrome values; and

means for comparing said expected syndrome values with said actual syndrome values.